

REMARKS

I. STATUS OF THE CLAIMS

Claims 9-10 are "objected to."

Claims 1-15 and 20-25 are currently pending. Of these claims, claims 12-15, 20, 22-23 and 25 are withdrawn from consideration.

II. OBJECTIONS

At page 2 of the Office Action, claims 1, 11, 21 and 24 are objected to as not having a relationship, "in the functional/structural between the two different current values." The claims have been amended to overcome the objection. It is respectfully submitted that the recitation of at least claim 1, "calculating current values of the power supply pads from the calculated current values between the nodes," is definite, and clear on its face. It is respectfully submitted the objection should be withdrawn.

At pages 2-3 of the Office Action, claims 1, 7-9, 11, 21 and 24 are objected to. The Office Action states the recitation, "adding or eliminating at least power supply pads in accordance with the result of the determination," has two different processes corresponding to two different conditions. The Applicants respectfully submit that the claims are clear and definite. Furthermore, the Examiner is reminded that claims only require that much detail which would appraise those of ordinary skill in the art of the embodiments contained therein. In view of the foregoing, the Applicants submit the objection should be withdrawn.

III. CLAIMS 1-8, 11-13, AND 20-25 ARE REJECTED UNDER 35 U.S.C. 102(E) AS BEING ANTICIPATED BY U.S. PATENT 6,523,150 BUFFET ET AL. ("BUFFET")

In the outstanding Office Action, the Office Action correlates, "determining whether the current value of each of the power supply pads exceeds the current capacity of the associated IO buffer" of claim 1 with Buffet, at: Fig. 4, step [205]; column 6, lines 1-5; Fig. 5, column 6, lines 13-25. Furthermore, the Office Action correlates the recitation, "eliminating or adding at least one power supply pad in accordance with the result of the determination" of claim 1 with Buffet, at: Fig. 4, step [210]; Fig. 11, steps [355] and [360]; column 6, lines 1-25 and Figs. 7-8. The Applicants respectfully disagree with the Office Action's assertions.

Buffet relates to a method of designing a voltage partitioned wirebond package. (See

Abstract). The Office Action fails to appreciate the recitation, "determining whether the current value of each of the power supply pads exceeds the current capacity of the associated IO buffer," of currently amended claim 1. Regarding the Office Actions correlations regarding the aforementioned recitation of claim 1, Buffet describes at Step 200 of Fig. 4, calculating IR drop in a chip voltage island. In other words, a voltage drop (voltage = current x resistance) is calculated.

Furthermore, the Applicants assertion is described in column 6, lines 4-9, which states that if the voltage drop is not acceptable, additional chip pads 125 are assigned as voltage island chip pads 125A, specifically as power pads assigned to either Vdd, Vddx or GND. Accordingly, the Applicants respectfully submit Buffet fails to describe determining whether the current value of each of the power supply pads exceeds the current capacity of the associated IO buffer as recited in currently amended claim 1 of the present application. Additionally, the Applicants were unable to find a description of an "associated IO buffer" within the cited portions of Buffet as related to the aforementioned recitation of currently amended claim 1 ("determining whether the current value of each of the power supply pads exceeds the current capacity of the associated IO buffer.")

Regarding the Office Actions correlations to "eliminating or adding at least one power supply pad in accordance with the result of the determination" of claim 1 of the present application, the Applicants respectfully disagree with the Office Action. At step 210 of Buffet, a calculated voltage drop computed in step 200 is not acceptable (by comparison to a voltage drop limit determined by the chip designer), then additional chip pads 125 are assigned as voltage island chip pads 125A, and if the calculated voltage drop computed in step 200 is acceptable, the method proceeds to steps 280 and 285 in FIG. 8. Further to the aforementioned description, the Applicants are unable to find a description of eliminating voltage island chip pads, and additionally, the cited portion of Buffet in step 205 describes the comparison to a voltage drop limit is determined by the chip designer. Accordingly, the Applicants respectfully submit Buffet fails to describe, "eliminating or adding at least one power supply pad in accordance with the result of the determination," as recited in currently amended claim 1.

Although the above comments are specifically directed to currently amended claim 1, for example, it is respectfully submitted that the comments would be helpful in understanding various differences of various other claims over the cited references.

In view of the above, it is respectfully submitted the rejection is overcome.

IV. CONCLUSION

There being no further outstanding objections or rejections, it is submitted that the application is in condition for allowance. An early action to that effect is courteously solicited.


Finally, if there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

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